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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,755	04/21/2004	Charles A. Miller	FACT-01005US0	5339

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EXAMINER	
NGUYEN, JIMMY	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,755	MILLER ET AL.	
	Examiner	Art Unit	
	Jimmy Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4, 6 - 9, 25 - 27, 33, 36, 37* is/are pending in the application.

4a) Of the above claim(s) *37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4, 6 - 9, 25 - 27, 33, 36,* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Argument

The examiner acknowledges the amendment filed 7/25/05 with the following effect;

Applicant's arguments with respect to claims 4, 6- 9, 25 –27, 33 and 36, 37 have been considered but are moot in view of the new ground(s) of rejection.

Restriction

1. Newly submitted claim 37 is directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: the method for testing DUTs using a probe card assembly is different invention with the probe card apparatus

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 37 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Drawings

The drawing filed 7/25/05 has been acknowledged and approved.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 4, 7, 28, 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Nachumovsky (US 2003/0074611 A1)

As to claims 4, 36, Nachumovsky disclose (fig 2) a the probe card assembly comprising a programmable controller (104) to control the provision of test signals to test probes (220) of the probe card for testing components on a wafer, (101) wherein the programmable controller (104) is connected through an interface (103, 201) to a test system controller (104), where the test system controller (104) provides test signals to the interface (103, 201) to control testing of components on a wafer (101), wherein the interface (103, 201) comprises one or more of a group consisting of wireless.

As to claim 7, Nachumovsky disclose (fig 1) a probe card assembly comprising a programmable controller (104) to control the provision of test signals to test probes of the probe card (102) for testing components (11) on a wafer (101), wherein programmable controller (104) is configured to perform self testing (150, column 2 lines 1 – 7) of components included in the probe card assembly (102).

As to claim 28, Nachumovsky disclose (fig 1) a probe card assembly comprising a programmable controller ((104)) configured to perform self testing (150, column 2 lines 1 – 7) of components included in the probe card assembly (102).

3. Claims 6, 8, 9, 29 - 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Lino et al (US 6,380,753)

As to claims 6, 8, 29, 30, Lino et al teach (fig 2) a probe card assembly comprising a programmable controller (13) to control the provision of test signals to test probes of the probe card (17) for testing components on a wafer (W), wherein the programmable controller (13) comprises a serial to parallel converter (31, 25) configured to receive the test signals (from 12), the programmable controller (13) configured to convert the test serial from serial to parallel (fan out the test signal) and distribute the test signals in parallel to the test probes and the serial to parallel converter.

As to claim 9, Lino et al teach (fig 2) the probe card assembly of claim 8, wherein the serial to parallel converter (31, 25) comprises a serial digital to analog converter (25) connectec to receive digital test signals from the programmable controller (21), the digital to analog converter (25) configured to convert the serial signals to parallel and to provide the test signals to the test probes in analog form.

As to claim 31, Lino et al teach (fig 2) the probe card assembly wherein the serial to parallel converter comprises a FPGA.

As to claims 32, 35, Lino et al teach (fig 2)

A space transformer (17) supporting the test probes;

at least one daughter card (13); and

a base PCB (15) electrically interconnected with the space transformer (17) and the at least one daughter card (13), wherein serial to parallel converter (31) , ADC (26), DCA (25) are provided on at least one daughter card (13).

As to claim 33, Lino et al teach (fig 2) a probe card assembly comprising:

a serial digital to analog converter (26) configured to serially receive digital test signal that are to be distributed to test probes of the probe card (13) in analog form the digital to analog converter (25) configured to convert the test signals to parallel and to provide the test signal to the test probes in analog form.

As to claim 34, Lino et al teach (fig 2) an ADC configured to receive an analog signal from a test device and to send a digital representation to a test system controller

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 25, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nelso et al (US 5,550,480) in view of Leas et al (US 6,351,134).

As to claim 27, Nelson et al disclose (fig 4) a probe card assembly comprising:

a DC-DC converter (Vref3, column 7 lines 11 – 16) connected (when the multiple probes contact with the wafer 16) between the single power supply line Vref4) of a test system controller (51), the power supply line (Vref4) distributing power through line branches to multiple test probes 25, 20), the DC-DC converter (Vref 3) configured to increase current in a signal provided on the power supply line;

However, Nelson et al are silent on a probe card assembly comprising:

power supply isolation devices connected in series with multiple power supply lines that distribute power from a single power supply line of a test system controller to multiple test probes, each test probe configured to contact a DUT power supply input, wherein the power supply isolation devices (40) are configured to minimize current flow on a given one of the power supply lines when a DUT on the given line is determined to be faulty,

On the other hand, Leas et al teach a probe card assembly comprising:

power supply isolation devices (40) connected in series with multiple power supply lines that distribute power from a single power supply line (PS) of a test system controller to multiple test probes, each test probe configured to contact a DUT power supply input, wherein the power supply isolation devices (40) are configured to minimize current flow on a given one of the power supply lines when a DUT (37) on the given line is determined to be faulty.

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the probe card assembly of Nelson et al with the isolation device of Leas et al for the purpose of regulating the power supply to device under test.

As to claim 25, Leas et al disclose (figs 1 and 2) the probe card assembly of claim 27, wherein the power supply isolation devices comprise one or more of a group consisting of voltage regulators (40, each DUT 37 has its own voltage regulators 40).

5. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nelso et al (US 5,550,480) in view of Leas et al (US 6,351,134) and further in view of Sporck et al (US 6, 856,150).

As to claim 26, the combination of Nelso et al and Leas et al disclose (figs 1 and 2) a probe card assembly comprising:
power supply isolation devices (40) connected in series with multiple power supply lines that distribute power from a single power supply line (PS) of a test system controller to multiple test probes, each test probe configured to contact a DUT power supply input, wherein the power supply isolation devices (40) are configured to minimize current flow on a given one of the power supply lines when a DUT (37) on the given line is determined to be faulty and a space transformer (16) supporting the test probes (31) the

power supply isolation devices (40) are provided on at least one of the space transformer (16).

However, Leas et al and Nelso et al are silent on

at least one daughter card; and

a base PCB electrically interconnected with the space transformer and the at least one daughter card, wherein the power supply isolation devices are provided on at least one of the space transformer, the base PCB, and the at least one daughter card.

On the other hand, Sporck et al teach (fig 4A)

at least one daughter card (432); and

a base PCB (402) electrically interconnected with the space transformer (406) and the at least one daughter card (432),

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the test system of Leas et al and Nelso et al with the daughter card of Sporck et al for the purpose of providing additional space on the probe card to allow for the use of larger probe head assemblies while not interfering with connections between the semiconductor tester and the probe card (column 3 lines 15 – 23).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen whose telephone number is (703) 306-5858. The examiner can normally be reached on M- Ffrom 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ramitez Nestor, can be reached on 571 – 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jimmy Nguyen

9/ 24/05

VINH NGUYEN
PRIMARY EXAMINER
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09/28/05